

Fig. 1 (1)

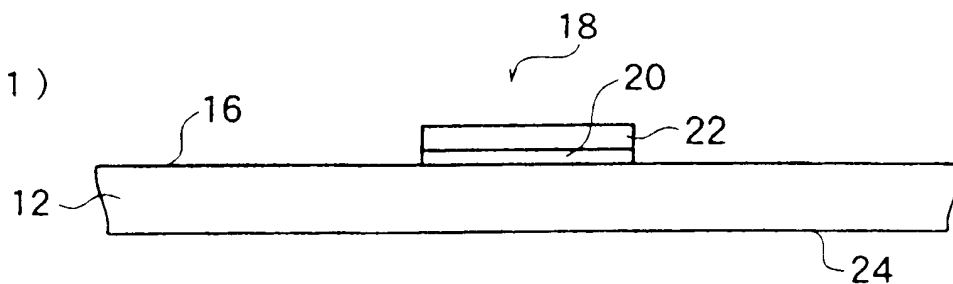


Fig. 1 (2)

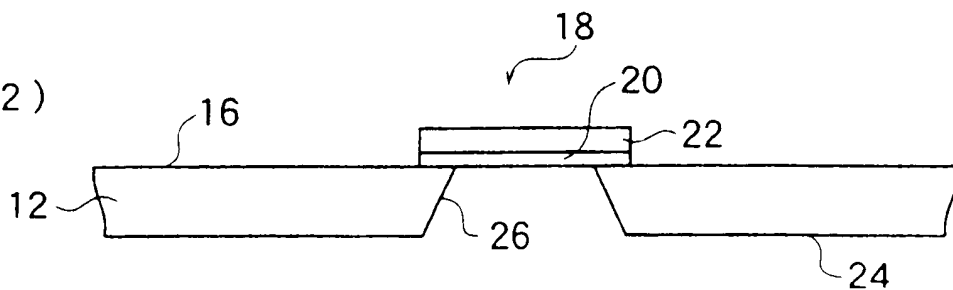


Fig. 1 (3)

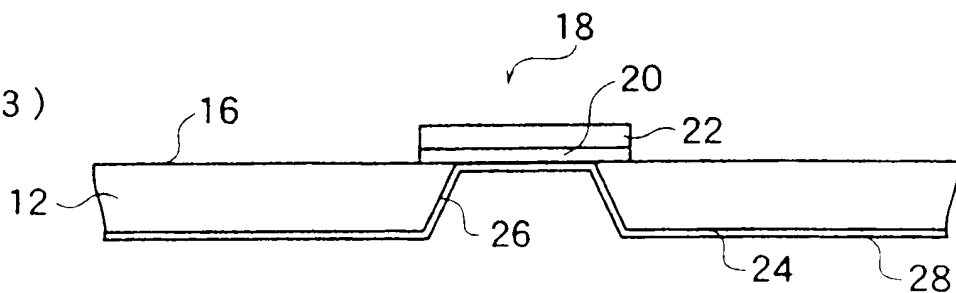


Fig. 1 (4)

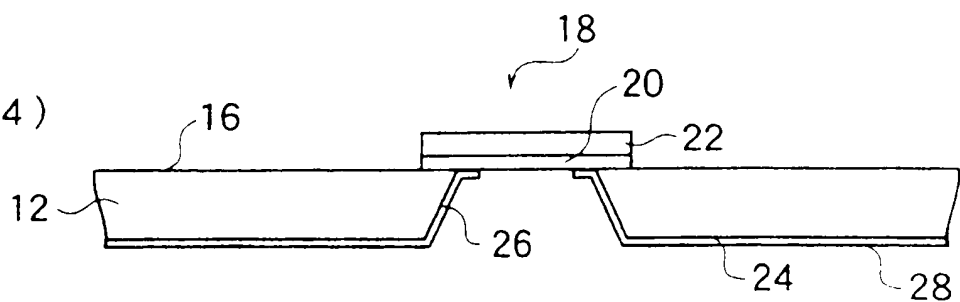


Fig. 2 (1)

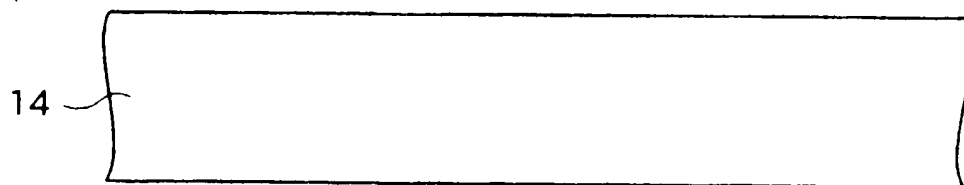


Fig. 2 (2)

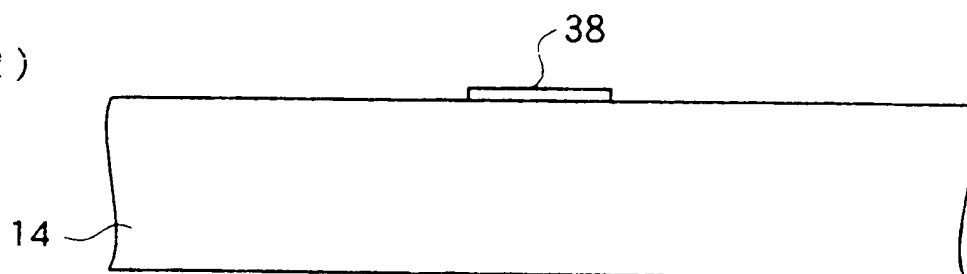


Fig. 2 (3)

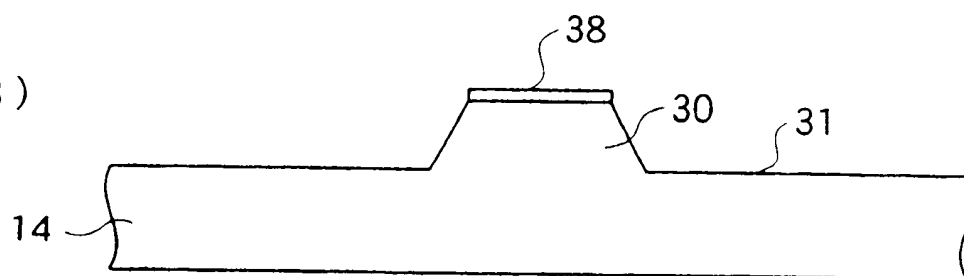


Fig. 2 (4)

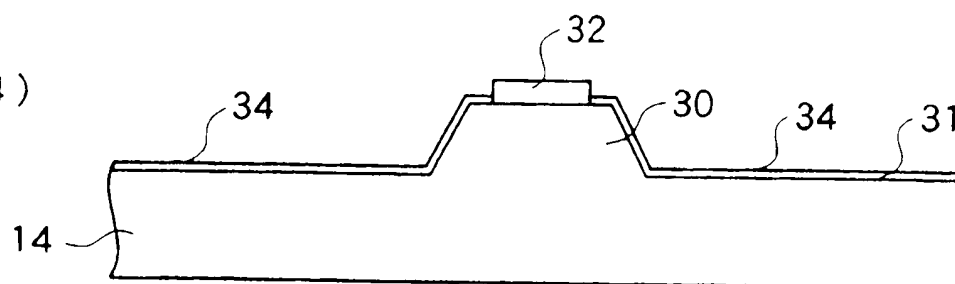


Fig. 3 (1)

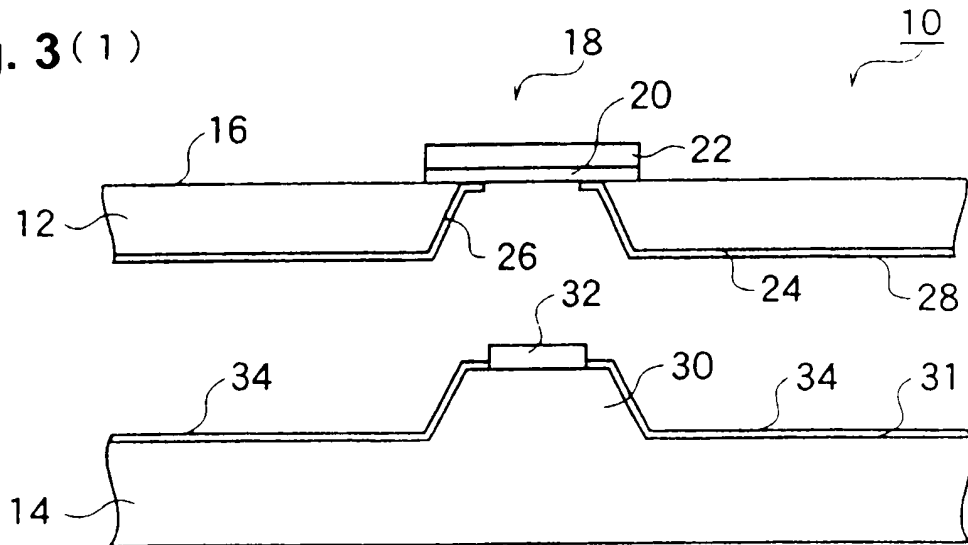
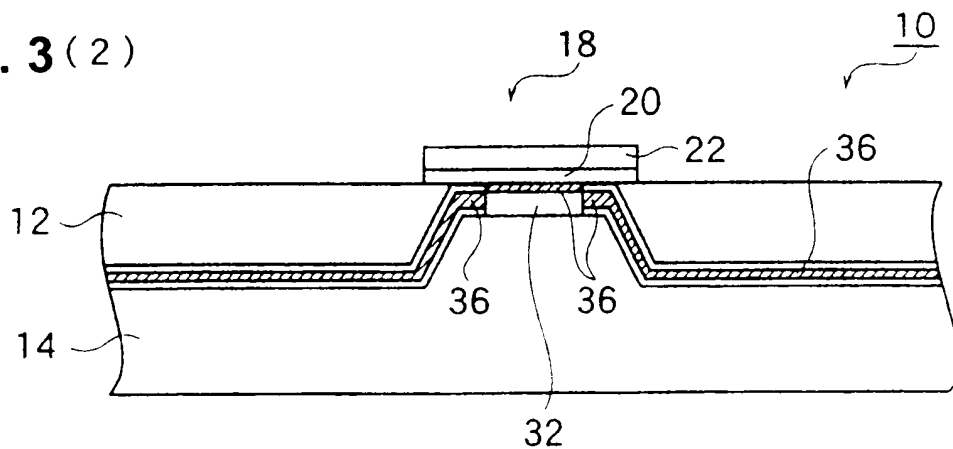


Fig. 3 (2)



- | | |
|--------------------------------|-------------------------|
| 10 : Semiconductor device | 16 : Surface |
| 12 : First semiconductor chip | 18 : Electrode |
| 14 : Second semiconductor chip | 32 : Abutting electrode |

Fig. 4 (1)

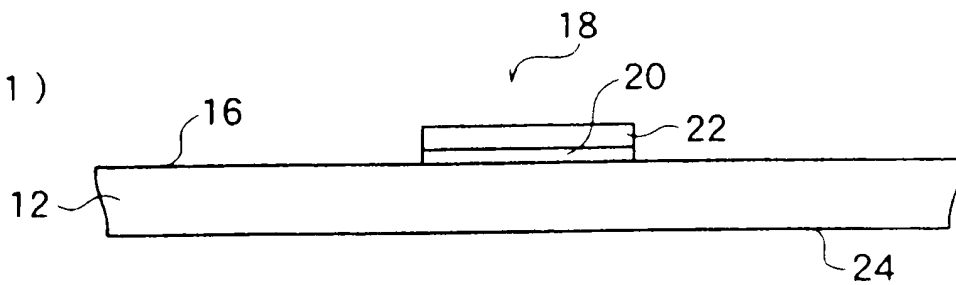


Fig. 4 (2)

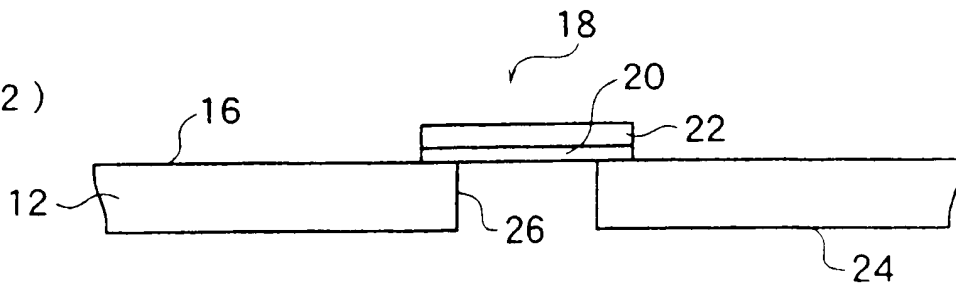


Fig. 4 (3)

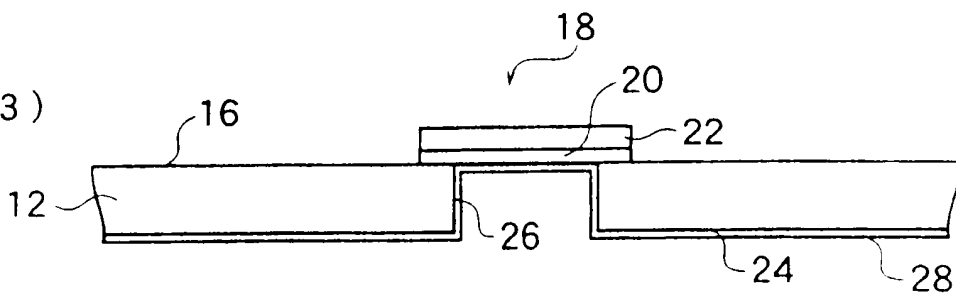


Fig. 4 (4)

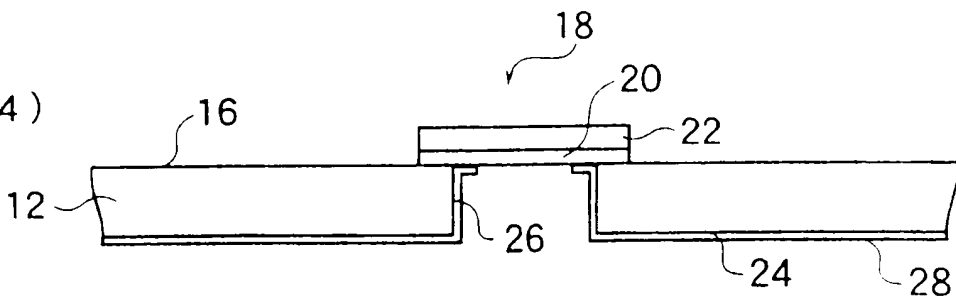
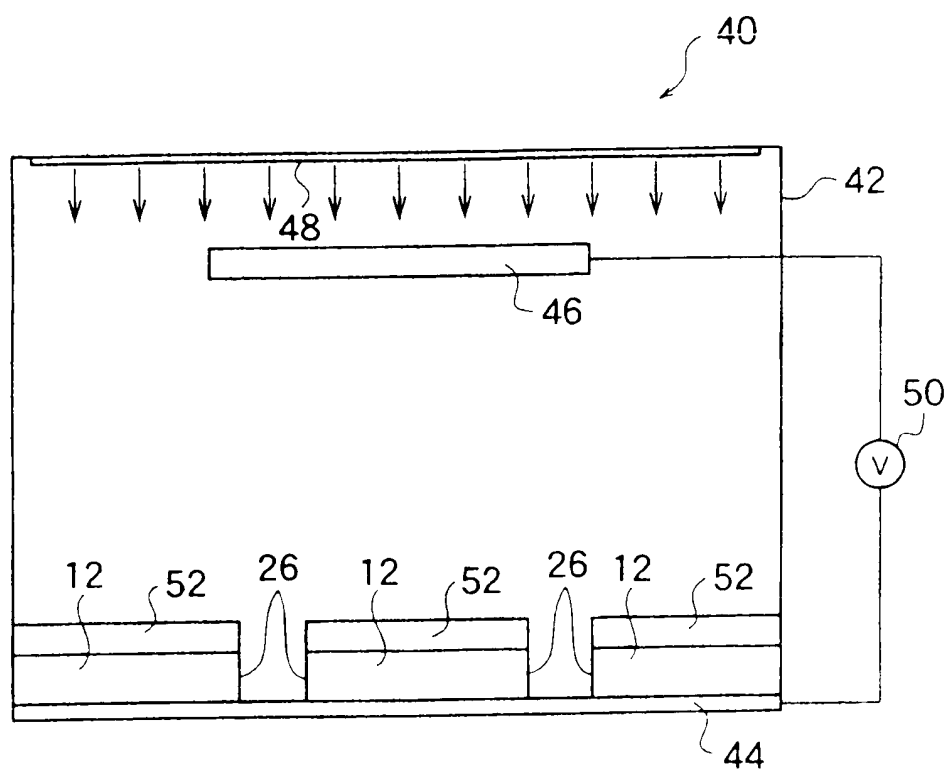
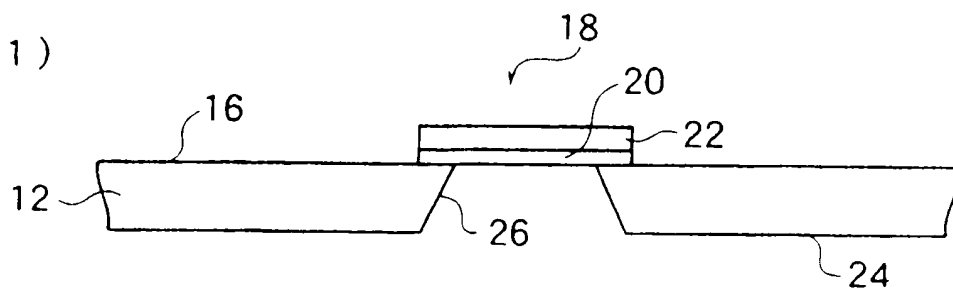


Fig. 5





2)

12, 16, 18, 20, 22, 24, 26, 28

This diagram shows a second embodiment of the device. It features a similar structure to the first embodiment, with a base (12) and a top layer (16). A central component (18) is positioned on top of the base, supported by a structure (20) that includes a layer (22). The base has a central recessed area (24) and side walls (26, 28).

